## IN THE CLAIMS

1. (Currently Amended) A method of operating a non-volatile memory device comprising:
coupling a precharge voltage through a substrate tub to a plurality of channels of a plurality of floating gate memory cells of ~~on a substrate tub of~~ a NAND architecture memory array ~~of a plurality of floating gate memory cells~~, wherein the plurality of floating gate memory cells are coupled in a plurality of strings;
coupling a gate programming voltage to the gate of a selected floating gate memory cell of each string of a selected number of strings; and
selectively coupling a program voltage or a program-inhibit voltage to a channel of each string of the selected number of strings.

2. (original) The method of claim 1, wherein the non-volatile memory device is one of a Flash memory device and a EEPROM memory device.

3. (original) The method of claim 1, wherein the gate programming voltage is approximately 20V.

4. (original) The method of claim 1, wherein the precharge voltage is approximately 5V.

5. (original) The method of claim 1, wherein the program voltage is approximately ground and the program-inhibit is approximately Vcc.

6. (original) The method of claim 1, further comprising:
coupling a pass voltage to the gates of one or more non-selected floating gate memory cells of each string of the selected number of strings.

7. (original) The method of claim 6, wherein the pass voltage level is approximately 10V.

8. (Currently Amended) The method of claim 1, wherein coupling the precharge voltage ~~on~~ through the substrate tub to the plurality of channels of the plurality of floating gate

memory cells and coupling the gate programming voltage to the gate of the selected floating gate memory cell of each string of the selected number of strings, further comprises coupling the precharge voltage ~~on~~ through the substrate tub to the plurality of channels of the plurality of floating gate memory cells and coupling the gate programming voltage to the gate of the selected floating gate memory cell of each string of the selected number of strings after uncoupling the precharge voltage.

9. (Currently Amended) The method of claim 1, wherein coupling the precharge voltage ~~on~~ through the substrate tub to the plurality of channels of the plurality of floating gate memory cells and coupling the gate programming voltage to the gate of the selected floating gate memory cell of each string of the selected number of strings, further comprises coupling the precharge voltage ~~on~~ through the substrate tub to the plurality of channels of the plurality of floating gate memory cells and coupling the gate programming voltage to the gate of the selected floating gate memory cell of each string of the selected number of strings before uncoupling the precharge voltage.

10. (Currently Amended) The method of claim 1, wherein coupling the precharge voltage ~~on~~ through the substrate tub to the plurality of channels of the plurality of floating gate memory cells and coupling the gate programming voltage to the gate of the selected floating gate memory cell of each string of the selected number of strings, further comprises coupling the precharge voltage ~~on~~ through the substrate tub to the plurality of channels of the plurality of floating gate memory cells and coupling the gate programming voltage to the gate of the selected floating gate memory cell of each string of the selected number of strings and uncoupling the precharge voltage after the gate programming voltage has reached a selected voltage level.

11. (original) The method of claim 10, wherein the selected voltage level is a gate programming voltage level of approximately 5V.

12. (original) The method of claim 1, wherein selectively coupling a program voltage or a program-inhibit voltage to a channel of each string of the selected number of strings

further comprises selectively coupling a program voltage or a program-inhibit voltage to a channel of each string of the selected number of strings through a drain select gate transistor.

13. (original) The method of claim 1, wherein selectively coupling a program voltage or a program-inhibit voltage to a channel of each string of the selected number of strings further comprises selectively coupling a program voltage or a program-inhibit voltage to a channel of each string of the selected number of strings when the gate programming voltage is coupled to the gate of the selected floating gate memory cell of each string of the selected number of strings.

14. (original) The method of claim 1, wherein selectively coupling a program voltage or a program-inhibit voltage to a channel of each string of the selected number of strings further comprises selectively coupling a program voltage or a program-inhibit voltage to a drain of a first floating gate memory cell of each string of the selected number of strings.

15. (original) The method of claim 1, wherein small feature low voltage circuit elements are used in a coupled bitline circuit and a coupled source line circuit.

16. (original) The method of claim 15, wherein the coupled bitline circuit has a decoder or a multiplexer.

17. (Currently Amended) A method of operating a non-volatile memory device comprising:
generating a channel of carriers in a selected plurality of floating gate memory cells of a memory array, where the memory cells are coupled in a plurality of strings by:
placing a precharge voltage on a substrate tub that is coupled to the memory array; and
programming a selected floating gate memory cell of a selected number of strings by:
removing the precharge voltage from the substrate tub,

placing a gate programming voltage on the control gate of the selected floating gate memory cell of the selected number of strings, and

selectively placing a program voltage or a program-inhibit voltage on a bitline coupled to a [[a ]]channel of each string of the selected number of strings.

18. (original) The method of claim 17, wherein the non-volatile memory device is one of a Flash memory device and a EEPROM memory device.

19. (original) The method of claim 17, further comprising:
placing a plurality of word lines coupled to a plurality of control gates of the selected plurality of memory cells in a high impedance state.

20. (original) The method of claim 17, further comprising:
placing a plurality of bitlines coupled to the plurality of strings in a high impedance state.

21. (original) The method of claim 17, further comprising:
placing at least one source line coupled to the plurality of strings in a high impedance state.

22. (original) The method of claim 17, further comprising:
placing approximately 4.5V on at least one source line coupled to the plurality of strings.

23. (original) The method of claim 22, wherein placing approximately 4.5V on at least one source line coupled to the plurality of strings further comprises placing 4.5V on at least one source line coupled to the plurality of strings through a plurality of source line gate transistors coupled to a source of a final floating gate memory cell of each string of the plurality of strings.

24. (original) The method of claim 17, further comprising:
placing approximately Vcc on at least one source line coupled to the plurality of strings.

25. (original) The method of claim 24, wherein Vcc is one of 3.3V and 1.8V.

26. (original) The method of claim 17, wherein programming a selected floating gate memory cell of a selected number of strings, further comprises:
placing a pass voltage on the non-selected floating gate memory cells of the selected number of strings.

27. (original) The method of claim 26, wherein placing a pass voltage on the non-selected floating gate memory cells further comprises placing an approximately 10V pass voltage on the non-selected floating gate memory cells.

28. (original) The method of claim 17, wherein programming a selected floating gate memory cell of a selected number of strings by placing a gate programming voltage on the control gate of the selected floating gate memory cell further comprises programming a selected floating gate memory cell of a selected number of strings by placing an approximately 20V gate programming voltage on the control gate of the selected floating gate memory cell.

29. (original) The method of claim 17, wherein generating a channel of carriers in a selected plurality of floating gate memory cells by placing a precharge voltage on a substrate tub further comprises generating a channel of carriers in a selected plurality of floating gate memory cells by placing an approximately 5V precharge voltage on a substrate tub.

30. (original) The method of claim 17, wherein programming a selected floating gate memory cell of a selected number of strings by removing the precharge voltage from the substrate tub further comprises removing the precharge voltage and bringing the substrate tub to a selected normal substrate tub voltage.

31. (original) The method of claim 17, wherein programming a selected floating gate memory cell of a selected number of strings by removing the precharge voltage from the

substrate tub further comprises removing the precharge voltage and grounding the substrate tub.

32. (original) The method of claim 17, wherein programming a selected floating gate memory cell of a selected number of strings by removing the precharge voltage from the substrate tub further comprises removing the precharge voltage from the substrate tub after placing the gate programming voltage on the control gate of the selected floating gate cell.

33. (original) The method of claim 32, wherein removing the precharge voltage from the substrate tub after placing the gate programming voltage on the control gate of the selected floating gate cell further comprises removing the precharge voltage from the substrate tub after the gate programming voltage reaches a selected voltage level.

34. (original) The method of claim 33, wherein the selected voltage level of the gate programming voltage is approximately 5V.

35. (original) The method of claim 17, wherein programming a selected floating gate memory cell of a selected number of strings by removing the precharge voltage from the substrate tub further comprises removing the precharge voltage from the substrate tub before placing the gate programming voltage on the control gate of the selected floating gate cell.

36. (original) The method of claim 17, wherein an erase circuit coupled to the substrate tub generates the precharge voltage.

37. (original) The method of claim 17, wherein low voltage circuit elements are used in a coupled bitline circuit and a coupled source line circuit.

38. (Currently Amended) A method of programming a NAND architecture floating gate memory cell string comprising:

precharging a channel of carriers in the NAND architecture floating gate memory cell string by coupling a precharge voltage to the NAND architecture floating gate memory string through a substrate that is coupled to the NAND memory string;

coupling a gate programming voltage to the gate of a selected floating gate memory cell of the string;

coupling a high pass voltage to the gates one or more non-selected floating gate memory cells of the string; and

selectively coupling a program voltage or a program-inhibit voltage to a channel of the string.

39. (Currently Amended) The method of claim 38, wherein precharging a channel of carriers in the NAND architecture floating gate memory cell string by coupling a precharge voltage to the NAND architecture floating gate memory string through a substrate that is coupled to the NAND memory string further comprises precharging a channel of carriers in the NAND architecture floating gate memory cell string by coupling a precharge voltage to the NAND architecture floating gate memory string through a substrate that is coupled to the NAND memory string by coupling ~~a~~ the precharge voltage to the NAND architecture floating gate string from a substrate tub.

40. (Currently Amended) The method of claim 38, wherein precharging a channel of carriers in the NAND architecture floating gate memory cell string by coupling a precharge voltage to the NAND architecture floating gate memory string through a substrate that is coupled to the NAND memory string and coupling a gate programming voltage to the gate of a selected floating gate memory cell of the string, further comprises precharging a channel of carriers in the NAND architecture floating gate memory cell string by coupling a precharge voltage to the NAND architecture floating gate memory string through a substrate that is coupled to the NAND memory string and coupling a gate programming voltage to the gate of a selected floating gate memory cell of the string after uncoupling the precharge voltage.

41. (Currently Amended) The method of claim 38, wherein precharging a channel of carriers in the NAND architecture floating gate memory cell string by coupling a precharge voltage to the NAND architecture floating gate memory string through a substrate that is coupled to the NAND memory string and coupling a gate programming voltage to the gate of a selected floating gate memory cell of the string, further comprises precharging a channel of carriers in the NAND architecture floating gate memory cell string by coupling a precharge voltage to the NAND architecture floating gate memory string through a substrate that is coupled to the NAND memory string and coupling a gate programming voltage to the gate of a selected floating gate memory cell of the string before uncoupling the precharge voltage.

42. (Currently Amended) The method of claim 38, precharging a channel of carriers in the NAND architecture floating gate memory cell string by coupling a precharge voltage to the NAND architecture floating gate memory string through a substrate that is coupled to the NAND memory string and coupling a gate programming voltage to the gate of a selected floating gate memory cell of the string, further comprises precharging a channel of carriers in the NAND architecture floating gate memory cell string by coupling a precharge voltage to the NAND architecture floating gate memory string through a substrate that is coupled to the NAND memory string and coupling a gate programming voltage to the gate of a selected floating gate memory cell of the string and uncoupling the precharge voltage after the gate programming voltage has reached a selected voltage level.

43. (original) The method of claim 38, wherein selectively coupling a program voltage or a program-inhibit voltage to a channel of the string, further comprises selectively coupling a program voltage or a program-inhibit voltage to a channel of the string when the gate programming voltage is coupled to the gate of the selected floating gate memory cell of the string.

44. (Currently Amended) A method of programming a NAND architecture floating gate memory cell array comprising:

applying a precharge voltage through a substrate tub to a plurality of channels of a plurality of floating gate memory cells ~~to a substrate tub~~ of the NAND architecture memory array, wherein the ~~NAND architecture memory array contains a~~ plurality of floating gate memory cells are serially coupled source to drain in a plurality of strings;

applying a programming voltage to a selected floating gate memory cell of each string of a selected number of strings;

applying a pass voltage to one or more non-selected floating gate memory cells of each string of the selected number of strings; and

selectively applying a program voltage to a drain of a channel of each string of the selected number of strings.

45. (original) The method of claim 44, wherein selectively applying a program voltage to a drain of a channel of each string of the selected number of strings, further comprises selectively applying a program voltage or a program-inhibit voltage to a drain of a channel of each string of the selected number of strings.

46. (Currently Amended) A method of programming a floating gate transistor memory cell comprising:

generating a channel of carriers in the floating gate transistor memory cell by coupling a precharge voltage to a channel region of the floating gate transistor memory cell through ~~on~~ a substrate tub the floating gate transistor memory cell is formed on;

coupling a gate programming voltage to the floating gate transistor memory cell of each string of a selected number of strings; and

coupling a program voltage or a program-inhibit voltage to the channel of the floating gate transistor memory cell.

47. (original) The method of claim 46, wherein the floating gate transistor is coupled in series to at least one additional floating gate memory cell.

48-84. (cancelled)